TEMIC

Digital Integration

Design done by
Customer and TEMIC

Introduction

When integrating the digital part of modern electronic system, various technical and financial criteria are considered.

Over 10 years of ASIC experience have shown that no methodology can meet them all in the same time. TEMIC experience at proposing its customers the most appropriate solution has become an art, resulting in long-term partnership.

Our customers/partners have themselves experienced several ways of doing ASICs, from the use of heavy internal investment with their own design centers, to the full sub-contracting to ASIC vendors from mere product specifications.

Know-how protection, engineering workload management and evolution of merchant CAD tools have been leader factors in the evolution of the preferred solutions.

The border between the own skills of equipment manufacturers and those of semiconductors makers has evolved : high level behavioral description -such as VHDL - has become the most appropriate language for users to bridge between system description and physical implementation.

On the other end, submicron electronics and faster digital systems have revealed new challenges to cope with the electrical behavior of signals, both on and outside the chip. For instance, clock or signal skews, cross-talks, noise, electromagnetic emission or susceptibility have become the main drivers of first-pass yields in design.

Testing of largely integrated systems -sometimes including processor cores- is also a matter of many trade-offs between circuit cost, development time and safety operation.

New generations of programmable devices such as CPLD or FPGA have also appeared, offering unbeatable flexibility and development time, but with many drawbacks in cost, sourcing , logistics, reliability, etc.

On top of the long experince of our designers, TEMIC has developed an unmatched choice of ASIC solutions offering the best trade-off in development or production cost, flexibility or performance.

Our solutions are also compatible with previous choices or vendor policies from our clients. On top of our proven capacity to deliver high-quality silicon devices in volume, we are recognized for helping them to find the way to secure their present or future supplies, while remaining competitive along the lifetime of their systems.

TEMIC is committed to help its clients to save time, money, while avoiding thrilling hassle.

Digital Integration

Design done by Customer and TEMIC

Introduction

For Arrays and Composite Array, Logic Design is done by Customer, using MHS libraries on supported tools. Customer will give to MHS a simulated netlist compliant with MHS Design Rules. MHS will perform the layout and give back a backannoted netlist for postlayout simulation. Design Review is signed when both parties agree on final simulation results.

Three physical implementations can be used by Customer : ULC, Array or Composite Array.

For ULCs, Customer gives FPGA or PLD code and two masters.

Universal Logic Circuits

This document presents an overview of ULC characteristics.For further information, ULC Databook can be provided upon request.

Description

FPGAs and PLDs are excellent tools for design development and lower-volume production. They provide a quick design cycle for fast time to market, low development costs and low risk. In higher-volume production, with proven and stable designs, where cost, quality, power consumption, and manu- facturablilty are important considerations, ULC™ devices are a preferred alternative with significant improvements in each of these characteristics.

ULCs (Universal Logic Circuits) are factory-customized circuits that are pin-for-pin drop-in replacements for a wide range of FPGAs and programmable logic devices. MHS has developed a proprietary design flow that enables ULC conversions to be completed on a turnkey basis in most cases. This design flow, called ***Verify-Before-Silicon***, allows MHS to validate the correctness of any conversion directly against the original FPGA or PLD design without requiring a time- consuming simulation signoff by the customer. ***Verify-Before-Silicon*** also means that for a proven FPGA or PLD design, MHS assumes the risk that the ULC conversion is correct, unlike the typical ASIC conversion process where the customer assumes all of the risk that it is correct by virtue of a simulation sign-off.

Features

- Mask Programmed drop-in replacements for Field-Programmable Gate Arrays (FPGAs) and Programmable Logic Devices (PLDs)
- Cost reduction for volume applications
  - 20%, 50%, even 75% or more is possible
  - Function of density, volume and speed
- Easy, low-cost, low-risk conversion
  - Turnkey conversion and verification
  - No simulation sign-off required
  - No NRE for standard commercial and industrial ULCs
  - Guaranteed to work in the application, rather than to simulation
  - No obligation if parts don't work in the application
- Quality improvement
  - Each ULC™ device tested for functional, dc and ac specifications
- Reduced power consumption
  - 85-95% reduction for most PLD and EPLD devices
- Wide range of architectures and speeds
  - 10- and 15-ns PLDs – 22V10, etc.
  - 10- through 20-ns EPLDs (MACH™, Altera® MAX®)
  - Most FPGAs (Xilinx™, Actel™, Altera®)
- Simplified manufacturing
  - Eliminates programming, testing or labeling
- Production flows available for most devices:
  - Commercial, Industrial and Military temperatures
  - Military and Radiation Tolerant flows

Verify-Before Silicon Technique

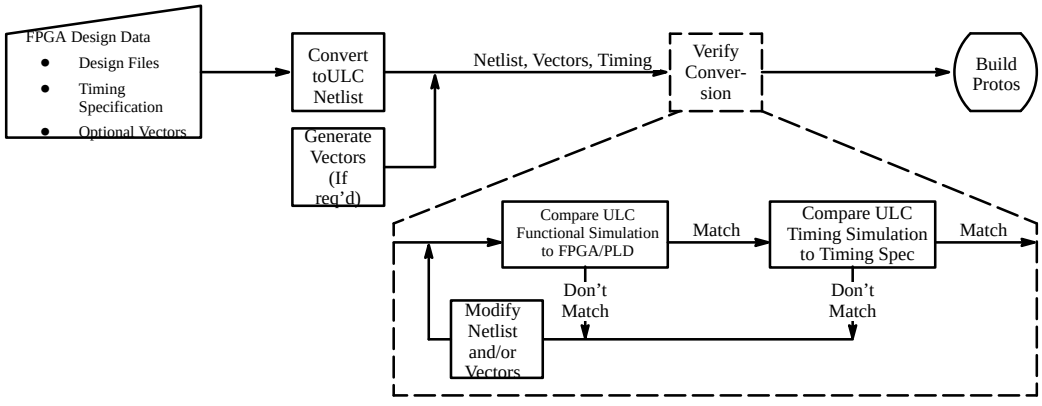

Figure 1. MHS Verify-Before-Silicon Process

ULCs combine the design-cycle advantages of FPGAs and PLDs, with the production advantages of an ASIC to provide the best of both worlds.

Technology

ULCs are manufactured with advanced sub-micron CMOS technology. Several different series are used to meet the constraints of different PLD and FPGA types as well as unique customer requirements. The UD series of ULCs uses 0.8-mm (drawn) single-level metal CMOS. The UC series uses 0.85-mm (drawn) double-level metal CMOS. These technologies offer toggle rates in excess of 200 MHz and input-output propagation delays as fast as 7 ns. They are designed for cost-effective volume production, and thus offer state-of-the-art performance combined with highly predictable and cost-effective manufacturability. The UD series has been in production since late 1988, and the UC series has been in production since 1989.

New for 1995 is the UG series of ULCs. This series uses 0.6-mm (drawn) double-metal or triple-metal CMOS. UG ULCs offer toggle rates up to 350 MHz and input-output propagation delays as fast as 5 ns.

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Requested Design File by Family

PAL, GAL & FPLD Files

❑Source Equations (.ABL, .CPL, .PDS files, etc)
❑.JED fuse file

ACTEL FPGA Files

❑.ADL files ❑.PIN file

ALTERA "Classic" (EP) Files

Parts designed with "Classic" software. See MAX EPLD checklist if designed with MAX2 software.

❑.ADF file ❑.LEF file
❑.JED file ❑.SCH schematic file

ALTERA MAX (EPM) EPLD Files

❑ All design files : .GDF, .POF, .TDF, .FIT, .RPT
❑ EDO EDIF netlist (if using MAX2 software)
❑.TBL sim file using Binary Radix with all pins (or test patterns in truth table format)

ATMEL ATV EPLD Files

❑.ABL file ❑.JED fuse file

LATTICE pLSI EPLD Files

❑.LDF file ❑.JED fuse file

LATTICE pLSI EPLD Files

❑.LDF file ❑.JED fuse file

XILING FPGA Files

❑.XNF netlist file (XNF created by LCA2XNF)
❑.LCA *post layout* file
❑.BIT downloadable file
❑.MCS downloadable file (created from .BIT)

Field Programmable Devices Supported

Architectures

A wide range of architectures and vendors are supported for conversions. This includes most 10- and 15-ns PLDs, such as 22V10, 26V12, and 20RA10. It includes MACH™ family of EPLDs from AMD®. From Altera®, conversions are supported on EP "Classic" EPLDs, MAX® EPM5000™, and EPM7000™ family EPLDs and the FLEX®EPF8000™ series of FPGAs. From Actel™, ACT1™, ACT2™ and ACT3™ FPGAs. From Xilinx™, XC2000™, XC3000™, and XC4000™ as well as the XC7000 family of EPLDs. Conversions are also supported for Lattice™ pLSI™ EPLDs and Quicklogic pASIC™ FPGAs.

The Risk-Free Solution

With no NRE in commercial applications, and MHS' guarantee to work in the application, ULCs truly are the **Risk-Free** solution to cutting high FPGA and EPLD costs. There is little effort required to prepare for the conversion. The customer simply identifies stable programs, sends in the completed design checklist(s), and prepares to enjoy the savings.

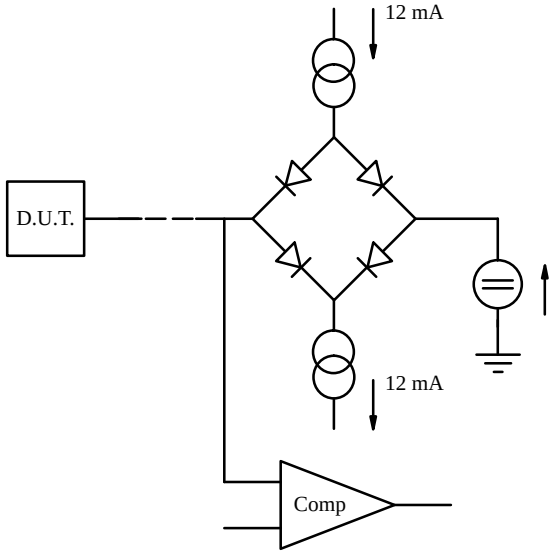
Typical ULC Test Conditions

For ac specification purposes, an improved output loading scheme has been defined for MHS high-drive (24 mA), high-speed ULC devices. The schematic below (Figure NO TAG) describes the typical conditions for testing these ULC devices, using the standard loading scheme commonly available on high-end ATE.

Compared to a no-load condition, this provides the following advantages:

- Output load is more representative of “real life” conditions during transitions.
- Transient energy is absorbed at the end of the line to prevent reflections which would lead to inaccurate ATE measurements.

The UD series of ULC™s is optimized for conversion of small- to medium-sized PLDs, CPLDs and FPGAs.



ULC

UD Series

Features

- High performance ULC™ family suitable for small to medium sized PLDs and FPGAs
- Conversions to approximately 8000 FPGA gates
- Pin counts to 100 pins
- Any pin-out matched due to no dedicated pads
- 0.8-mm (drawn)/0.65-mm (effective) single-layer metal CMOS technology
- All inputs incorporate a Schmitt trigger (0.4-V hysteresis) for improved noise immunity
  - Up to 48 mA of sink/source current per output pin with parallel output buffers
- Full range of packages: DIPs, SOICs, LCCs/PLCCs, PQFPs/TQFPs, PGAs/PPGAs
- Unique built-in voltage translation allowing mixed voltage operation:
  - 0- to 5-V input voltage allowed on all inputs and I/Os when operating at 3.3 V
  - No input clamping before 7-V Minimum
  - Offers voltage level translation when interfacing between 5-V and 3.3-V logic

Product Outline

Part Number	Pads	Equivalent FPGA Gates	Maximum Drive
UD02	31	750	24 mA
UD03	25	800	24 mA
UD09	51	2800	24 mA
UD10	68	3100	12 mA
UD14	78	4100	24 mA
UD16	84	4700	12 mA
UD27	100	8400	24 mA

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . –0.3 V to 7.0 V
Input Voltage (V_{IN}) . . . . . –0.3 V to 7.0 V
Storage Temperature . . . . . –65 to 150°C

Recommended Operating Range

V_{DD} . . . . . 5 V ±5% or 3.3 V ±5%
Operating Temperature
Commercial . . . . . 0 to 70°C
Industrial . . . . . –40 to 85°C
Military . . . . . –55 to 125°C

External Timing Characteristics

(Over the Operating Range)

These timing parameters are provided for information only. Actual pin-to-pin timing characteristics guaranteed for ULCs are determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed to separately by MHS.

Parameter	Symbol	Test Conditions	Min	Max		Unit
				Typ NO TAG	Max	
Propagation Time	t_{PD}	UD02		7.0	11.5	ns
		UD03		7.0	11.5	
		UD09		8.0	13.0	
		UD10		8.0	13.0	
		UD14		9.0	14.5	
		UD16		9.0	14.5	
		UD27		10.0	16.0	
Clock Delay Time	t_{CO}	UD02		8.0	13.0	
		UD03		8.0	13.0	
		UD09		10.0	16.0	
		UD10		10.0	16.0	
		UD14		12.0	19.5	
		UD16		12.0	19.5	
		UD27		14.0	22.5	
Hold Time	t_H		0.0			
Output Enable Time	t_{EN}	UD02		8.0	13.0	
		UD03		8.0	13.0	
		UD09		10.0	16.0	
		UD10		10.0	16.0	
		UD14		12.0	19.5	
		UD16		12.0	19.5	
		UD27		14.0	22.5	

ULC

UC Series

The UC series of ULC™s is well suited for converting medium- to large-sized CPLDs and FPGAs.

Features

- High-performance ULC family suitable for medium- to large-sized CPLDs and FPGAs
- Conversions to approximately 75,000 FPGA gates
- Pin counts to 240 pins
- Any pin-out matched due to limited number of dedicated pads
- 0.85-mm (drawn)/0.65-mm (effective) dual-layer metal CMOS technology
- High current drive capability on each I/O
  - Sink/source current up to 24 mA per buffer (commercial), 12 mA (industrial, military)
- Full range of packages: DIP, SOIC, LCC/PLCC, PQFP/TQFP, PGA/PPGA
- 3.3-V to 5-V operation
- Low quiescent current: 0.4 nA/gate
- Available in commercial, industrial, automotive, military and space grades
- Slew rate controlled output buffers

Product Outline

Part Number	Pads	Equivalent FPGA Gates	Maximum Bits RAM
UC04	32	1000	N/A
UC08	44	2100	N/A
UC2	68	5000	N/A
UC5	88	10000	500
UC8	128	14000	850
UC10	128	18000	1100
UC12	160	20000	1300
UC22	148	30000	1850
UC29	200	40000	2500
UC35	184	48000	4300
UC50	220	60000	5700
UC66	292	75000	7500

The “Max Bits RAM” column listed in the Product Outline table details the maximum amount of Xilinx XC4000 style RAM (16 X 1 blocks etc.) that could be implemented in each matrix if all of the cells were used for RAM. In an actual circuit, some of the cells would be required to implement logic, so the actual amount of RAM would need to be reduced to accommodate the logic.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . –0.5 V to 7.0 V
Input Voltage (V_{IN}) . . . . . –0.5 V to V_{DD} + 7.0 V
Storage Temperature . . . . . –65 to 150°C

Recommended Operating Range

V_{DD} . . . . . 5 V ±5% or 3.3 V ±5%
Operating Temperature
Commercial . . . . . 0 to 70°C
Industrial . . . . . –40 to 85°C
Military . . . . . –55 to 125°C

External Timing Characteristics

(Over the Operating Range)

These timing parameters are provided for information only. Actual pin-to-pin timing characteristics guaranteed for ULCs are determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed to separately by MHS.

Parameter	Symbol	Test Conditions	SSO	Min	Max		Unit
					Typ NO TAG	Max	
Propagation Time	t_{PD}	UC04, UC08			9.0	14.0	ns
		UC2			11.0	18.0	
		UC5			11.0	18.0	
		UC8, UC10			12.0	19.0	
		UC12, UC22			12.0	19.0	
		UC29, UC35			13.0	21.0	
		UC50, UC66			15.0	24.0	
Clock Delay Time	t_{CO}	UC04, UC08	32		11.0	18.0	
		UC2	52		13.0	21.0	
		UC5	64		13.0	21.0	
		UC8, UC10	100		15.0	24.0	
		UC12, UC22	124		15.0	24.0	
		UC29, UC35	164		27.0	27.0	
		UC50, UC66	200		20.0	32.0	
Hold Time	t_H			0.8			
Output Enable Time	t_{EN}	UC04, UC08	32		9.0	14.0	
		UC2	52		11.0	18.0	
		UC5	64		11.0	18.0	
		UC8, UC10	100		13.0	21.0	
		UC12, UC22	124		13.0	21.0	
		UC29, UC35	164		15.0	24.0	
		UC50, UC66	200		18.0	29.0	

ULC

UG Series (Preliminary)

The UG series of ULC™s is well suited for conversion of medium- to-large sized CPLDs and FPGAs.

Features

- High performance ULC family suitable for medium- to large-sized CPLDs and FPGAs
- Conversions to over 200,000 FPGA gates
- Pin counts to over 300 pins
- Any pin-out matched due to limited number of dedicated pads
- Advanced 0.6-mm (drawn)/0.45-mm (effective) feature size
- Triple-layer or dual-layer metal CMOS technology
- High speed performance:
  - 250-ps typical cell delay
  - 350-MHz toggle rate
- Full range of packages: DIP, SOIC, LCC/PLCC, PQFP/TQFP, PGA/PPGA
- 3-V to 5-V operation.
- Low quiescent current: 0.4 nA/gate
- Available in commercial, industrial, automotive, military and space grades.
- Slew rate and noise controlled output buffers

Product Outline

Part Number	Pads	Equivalent FPGA Gates	Maximum Bits RAM
UG00	24	1800	N/A
UG01	32	3300	N/A
UG02	36	4200	180
UG04	48	7500	310
UG09	72	15800	790
UG14	88	24300	1210
UG20	104	34800	1740
UG33	130	46000	2880

Part Number	Pads	Equivalent FPGA Gates	Maximum Bits RAM
UG42	146	58600	3660
UG52	162	63700	4550
UG70	188	85800	6130
UG90	212	108500	7750
UG120	244	145100	10360
UG140	264	156800	12250
UG200	312	206300	17190

The “Max Bits RAM” column listed in the Product Outline table details the maximum amount of Xilinx XC4000 style RAM (16 x 1 blocks etc.) that could be implemented in each matrix if all of the cells were used for RAM. In an actual circuit, some of the cells would be required to implement logic, so the actual amount of RAM would need to be reduced to accommodate the logic.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . –0.5 V to 7.0 V
Input Voltage (V_{IN}) . . . . . –0.5 V to V_{DD} + 7.0 V
Storage Temperature . . . . . –65 to 150°C

Recommended Operating Range

V_{DD} . . . . . 5 V ±5% or 3.3 V ±5%
Operating Temperature
Commercial . . . . . 0 to 70°C
Industrial . . . . . –40 to 85°C
Military . . . . . –55 to 125°C

External Timing Characteristics

(Over the Operating Range)

These timing parameters are provided for information only. Actual pin-to-pin timing characteristics guaranteed for ULCs are determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed to separately by MHS.

Parameter	Symbol	Test Conditions	SSO	Min	Max		Unit
					Typ NO TAG	Max	
Propagation Time	t_{PD}	UG00–02			5.0	7.5	ns
		UG04–UG09			6.0	9.0	
		UG14–UG20			7.0	10.5	
		UG33–UG90			8.5	13.0	
		UG120–UG200			9.5	14.5	
Clock Delay Time	t_{CO}	UG00–02	32		6.5	10.0	
		UG04–UG09	50		7.5	11.5	
		UG14–UG20	100		8.5	13.0	
		UG33–UG90	220		10.0	15.0	
		UG120–UG200	300		11.0	16.5	
Hold Time	t_H			0.0			
Output Enable Time	t_{EN}	UG00–02	32		6.5	10.0	
		UG04–UG09	50		7.5	11.5	
		UG14–UG20	100		8.5	13.0	
		UG33–UG90	220		10.0	15.0	
		UG120–UG200	300		11.0	16.5	

MG2 0.5µm CMOS Sea of Gates (Under Development)

Description

MG2 Sea of Gates are CMOS 0.5 micron, 3 metal layers channeless arrays, under development. MG2 will be available by mid 1997.

Targeted Features

- CMOS 0.5 micron, 3 metal layers
- 3V ± 10% or 3.3V ± 10% operating voltage
- Versatile I/O configuration : input, output, three-state, bidirectional, VCC, GND
- CMOS/TTL/GTL/PCI... interface
- Low power Consumption : 0.5µw/cell/MHz (worstcase industrial range)
- ESD (2kV) and latch-up protected I/O
- On chip Power on Reset, 250 MHz PLL, RC or Crystal oscillators
- RAM, DPRAM, FIFO compilers
- Wide range of Packages including BGA, PLCC, PQFP, SSOP, CPGA, CQFP, CLCC, Wafer and Die
- EDIF and VHDL Reference Formats
- Cadence, Compass, Mentor, Synopsis Reference Platforms
- Full compatibility with future MG2M Composite Sea of Gates
- Upward Compatibility with previous series

MG1 0.6 µm CMOS Sea of Gates

This document presents an overview of MG1 Series characteristics.
For further information, a full datasheet can be provided upon request.

Description

The MG1 sea of gates are CMOS 0.6 micron, 3 metal layers, channel–less array series ranging from 1k cell up to 500k cells.

MG1 basic cell provides high routability of logic with eAtremely dense compiled memories : ROM, RAM and DPRAM. For instance, the largest array is capable of integrating 128K bits of DPRAM with 128K bits of ROM and over 200,000 random gates.

Accurate control of clock distribution can be achieved by PLL hardware and CTS (Clock Tree Synthesis) software. New noise prevention techniques are applied in the array and in the periphery : Three or more independent supplies, internal decoupling, customisation dependent supply routing, noise filtering, skew controlled I/Os, low swing differential I/Os, all contribute to improve the noise immunity and reduce the emission level.

MG1 is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Cadence, Mentor, Synopsys and VHDL are the reference front end tools. Floor planning associated with timing driven layout provides a short back end cycle.

Features

- RAM, DPRAM, FIFO Compilers (2000 DPRAM bits per $mm^{2)}$
- Library Optimised for Synthesis, Floor Plan & Automatic Test Generation (ATG)
- High Speed Performances :
  – 250 ps Typical Gate Delay
  – 350 MHz Toggle Frequency
- High System Frequency Skew Control :
  – 250 MHz PLL for Clock Generation
  – Clock Tree Synthesis Software
- 3 & 5 Volts Operation; Single or Dual Supply Modes
- Low Power Consumption :
  – 0.9 µW/Gate/MHz @3 V
  – 2.4 µW/Gate/MHz @5 V
- Integrated Power on Reset
- Versatile I/O Cell : Input, Output, Bidirectionnal, Supply, Oscillator
- Standard 12mA I/Os, parallelism up to 48 mA
- ESD (2 kV) and Latch-up Protected I/O
- CMOS / TTL / pseudo ECL / GTL / PCI Interface
- High Noise & EMC Immunity :
  – I/O with Slew Rate Control
  – Internal Decoupling
  – Signal Filtering between Periphery & Core
  – Application Dependent Supply Routing & Several Independent Supply Sources
- Wide Range of Packages Including CPGA, CQFP, SOIC, PLCC , CLCC, PQFP, Wafer, Die
- Advanced CAD Support : Floor Plan, Proprietary Delay Models, Timing Driven Layout, Power Management
- Cadence, Compass, Mentor, Synopsys Reference Platforms
- EDIF & VHDL Reference Formats
- Upward Compatibility With MC & MF Gate Arrays, MCM & MFM Composite Arrays.
- Full Compatibility with MG1M Composite Sea of Gates Series
- Available In Commercial, Industrial, Automotive, Military & Space Quality Grades
- Special Versions on Radiation Tolerant Process

Product Outline

TYPE**	TOTAL CELLS	MAA USABLE CELLS	MAAIMUM PROGRAM-MABLE I/Os ***
MG1001	1 829	1 480	32
MG1004	3 608	3 420	48
MG1009	9 030	8 100	72
MG1014	13 846	12 000	88
MG1033	32 984	26 000	130
MG1042 *	42 000	35 700	146
MG1052	52 104	44 100	162
MG1070	70 059	57 900	188
MG1090 *	89 162	70 000	212
MG1120	118 472	88 900	244
MG1140 *	140 049	105 000	264
MG1265 *	264 375	185 100	360
MG1480 *	480 255	336 200	484

* Must be used when ceramic package is mandatory.
** Some matrices may not be available in military and space grades. Some other matrices may be developed on request.
*** I/O pads may be configured as VDD or VSS supplies according to circuit requirements

Libraries

The MG1 cell library has been designed to take full advantage of the features offered by both logic and test synthesis tools.

Cell / Macrocells libraries

5 and 3 Volt libraries can be delivered.

Macros library

Design testability is assured by the full support of SCAN, JTAG and BIST methodologies.

Block Generators

Block generators are used to create a customer specific simulation model and metallisation pattern for regular functions like RAM, DPRAM and FIFO. The basic cell architecture allows one bit per cell for RAM and DPRAM. The main characteristics of these generators are summarized below.

Function	MaAimum Size (bits)	bits/word	Typical characteristics (16 k bits)		
			typical access time (ns)	consumption (mA/MHz)	Used cells
RAM	72 k	1-144	8	1.6	20 k
DPRAM	72 k	1-144	8	3.3	23 k
FIFO	72 k	1-144	8	2.1	23 k

I/O Libraries

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator is located close to each buffer.

Inputs

Input buffers with CMOS or TTL thresholds are non inverting and feature versions with and without hysteresis. The CMOS and TTL input buffers may incorporate pull-up or pull down resistors. For special purposes, a buffer allowing direct input to the matrix core is available. A differential input buffer is also available allowing resolution of data values on small swing busses such as GTL or other proprietary solutions.

Differential input typical characteristics			
Supply (V)	**Differential voltage (mV)**	**Tphl (ns)**	**Tplh (ns)**
5	100	2,3	5,5
3	100	3,7	5,2

Outputs

Several kinds of CMOS and TTL output drivers are offered : fast buffers with 3, 6, 12 and 24 mA drive, low noise buffers with 12 mA drive. GTL and pseudo ECL bus drivers are also available.

Clock generation & PLL

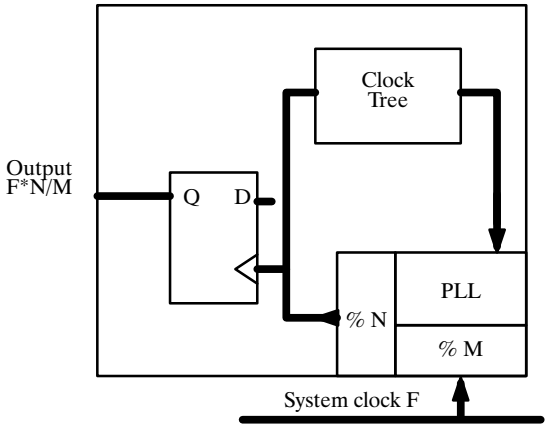
Clock generation

TEMIC / MHS offers 4 different types of oscillators : low power 32KHz crystal oscillator, high frequency crystal oscillator and 2 RC oscillators. For all devices, the mark-space ratio is better than 40/60 and the start-up time less than 10 ms; the other characteristics are summarized below :

	Frequency (MHz)		**Typical consumption (µA)**
	Minimum	**Maximum**	
xtal 32K	0.03	0.034	50
xtal 50 M	2	50	1 000
RC 10M	0.02	10	600
RC 32 M	10	32	1 500

PLL

Two independent PLL devices are located in upper left and lower right corners. Each may be used for the following functions :



The maximum frequency at PLL input after division by M is 70 MHz.

The maximum internal clock frequency is 250 MHz at 5 V and 150 MHz at 3 V; the minimum frequency is 20 MHz.

AC Characteristics examples

Specified at VDD = +5 V, TJ = 25°C, Process typical (all values in ns)

Description	Transition	Load (pf)		
		20	40	60
Output buffer with 12 mA drive	Tplh	1.85	2.69	3.54
	Tphl	1.45	1.82	2.19

Description	Transition	Standard Loads		
		2	5	10
2-Input NAND gate	Tplh	0.31	0.49	0.78
	Tphl	0.19	0.27	0.41

Specified at VDD = +3 V, TJ = 25°C, Process typical (all values in ns)

Description	Transition	Load (pf)		
		20	40	60
Output buffer with 12 mA drive	Tplh	3.05	4.44	5.84
	Tphl	2.39	3.00	3.61

Description	Transition	Standard Loads		
		2	5	10
2-Input NAND gate	Tplh	0.40	0.65	1.07
	Tphl	0.27	0.39	0.59

Propagation delays

Propagation delays for MG1 cells and blocks are a function of several factors including fan out, signal slope, interconnection capacitance, supply voltage, junction temperature and process tolerance and additionaly total irradiation dose for special operating conditions.

Propagation delays are provided for MG1 cells under nominal conditions (Tj = 25°C, VDD = 5.0 or 3.0 V, typical process, no irradiation). Worst case values are obtained by applying derating coefficients for temperature, voltage, process and total dose irradiation : KT, KV KP and KD. These coefficients are also design dependent and in the design kits each cell has its individual set of parameters.

Worst case propagation delays can however be estimated by using the following formula and tables :

Worst case = Typical * KTmax * KVmax * KPmax (* KDmax)

Voltage	KV
4.5	1.1
5	1
5.5	0.95

Process	KP
Best	0.82
Typical	1
Worst	1.28

Voltage	KV
2.7	1.15
3	1
3.3	0.89
3.6	0.81

Temperature	KT
–55	0.75
–40	0.79
0	0.92
25	1
100	1.24
115	1.29
145	1.38

Dose (krad)	KD
0	1
tbd	tbd

Absolute Maximum Ratings

Ambient temperature under bias (TA)

Commercial . . . . . 0°C to +70°C
Industrial . . . . . –40 to +85°C
Automotive . . . . . –40 to +125°C
Military . . . . . –55 to +125°C
Maximum Junction temperature . . . . . 150°C
Storage temperature . . . . . –65 to + 150°C

TTL/CMOS :

Supply voltage VDD . . . . . –0.5 V to +7 V
I/O voltage . . . . . –0.5 V to VDD + 0.5 V

Stresses at or above those listed may cause permanent damage to the device. Exposure to absolute maAimum rating conditions for extended period may affect device reliability.

Ordering Information

Consult your TEMIC sales office.

MG Matrix/Package Availability

Package Type	Pins	Width	Lead Spacing	MG													
				1001	1004	1009	1014	1033	1042	1052	1070	1090	1120	1140	1200	1265	1350	1480
SO	8		0.05	I														
	16		0.05	A														
	18		0.05	A	A													
	20		0.05	A	A													
	24		0.05	A	A													
	28		0.05	A	A													
PLCC J LEADED	28	0.45	0.05	A	A	A												
	44	0.65	0.05	A	A	A	A	A	A	A	A							
	68	0.95	0.05		A	A	A	A	A	A	A	A	A					
	84	1.15	0.05		A	A	A	A	A	A	A	A	A	A	A			
PQFP	44	10x10	0.8	A	A	A	A	A	A									
	52				I	I	I	I	I									
	64				I	A	I	I	I	I								
	80	14x20	0.8		A	A	A	A	A	A	A							
	100	14x20	0.65				A	A	A	A	A	A	A	A	A			
	128	28x28	0.8					A	A	A	A	A	A	A	A	A		
	160	28x28	0.65							A	A	A	A	A	A	A	A	
	208	28x28	0.5								A	A	A	A	A	A	A	A
	240											P	P	A	P	P	P	P
Power QUAD	80						I	I	I	I	I	I						
	100	14x20	0.65							A	A	A	A					
	128	28x28	0.8							A	A	A	A			A		
	144	28x28	0.65							P	P	P	P	P	P	P	P	P
	160	28x28	0.65							P	P	P	P	P	P	P	P	P
	208	28x28	0.5								P	P	P	P	P	A	P	P
	240	32x32	0.5									P	P	P	P	A	P	P
	304	40x40	0.5										P	P	P	P	P	P
TQFP (1.4mm max)	44	10x10	0.8	A	A	A	A	A	A									
	52				I	I	I	I	I									
	64	10x10	0.5		I	I	I	I	I	I								
	80	14x14	0.65				I	I	I	I	I	I						
	100	14x14	0.5							A	A	A	A					
	128	20x20	0.5							A	A	A	A					
	144	20x20	0.5							P	P	P	P	P	P	P	P	P
	160	28x28	0.65							P	P	P	P	P	P	P	P	P

A : Available. Contact MHS to check the pin out.
I : Introduction in progress (check for availability).
P : Planned

MG1 Matrix/Package Availability for Military and Space

Package	MG1014(E)	MG1042(E)	MG1090(E)	MG1140(E)	MG1265(E)	MG1480
PGA391					I*	I*
PGA340					I*	I*
PGA299				I*	I*	I*
PGA256				A*	A*	A*
PGA209			A*	A*	A*	A*
PGA180		A*	A*	A*	A*	A*
PGA176		A*	A*	A*	A*	A*
PGA144		A*	A*	A*	A*	
PGA132		A*	A*	A*	A*	
PGA120		A*	A*	A*		
PGA100	A*	A*	A*	A*		
PGA84	A*	A*	A*			
PGA68	A*	A*				
MQFPL196			A	A	A	A*
MQFPL160		A	A	A	A	
MQFPL132		A	A	A	A	
MQFPL100	A	A	A	A		
MQFPL80	A	A	A			
MQFPL68	A	A				
MQFPF340					I	I*
MQFPF304				I	I	I*
MQFPF256				A	A	A*
MQFPF196			A	A	A	A*
MQFPF172		A	A	A	A	
MQFPF160		A	A	A	A	
MQFPF132		A	A	A	A	
MQFPF100	A	A	A	A		
MQFPF84	A	A	A			
LCC100	A	A	A	A		
LCC84	A	A	A			
LCC68	A	A				
LCC44	A					
MQFPJ84	A	A	A			
MQFPJ68	A	A				
MQFPJ44	A					
CERDIP48	A*					
CERDIP40	A*					
SB64	A	A				
SB48	A					
SB40	A					

A : available
I : Introduction in progress (check for availability)
* : for military grade only

MG1RT : Radiation Tolerant 0.6µm CMOS Sea Of Gates

Description

TEMIC / MATRA MHS is the first European supplier for space application submicronic radiation tolerant CMOS ASICs.

This is why TEMIC keeps offering a fluent way of moving up and down the quality and the space/radiation tolerant capability of its products offering, and makes available its advance submicronic CMOS MG1 sea of gates family, through a mask compatible space / radiation tolerant process, so called "MG1RT" : this is the result of the TEMIC "Dual Use Technology" strategy serving the AMS (Avionics, Military & Space) market segments.

It offers the user to either go directly to a radiation tolerant prototypes and flight models delivery, or to start with cheaper non radiation tolerant prototypes, converting, then, to the radiation tolerant version, only when EQM or FM are actually needed, provided proper simulations have been run before going either way.

Features

- mask compatible radiation tolerant version of the MG1 gate arrays family
- total dose capability, when tested at 1600 rad/h :
  - better than 100 Krads for functionality
  - better than 50 Krads for first stand by current drift
- no rebound effect demonstrated after annealing
- positive influence of space very low dose rate (< 1 rad/h) expected
- latch up free : better than 100 MeV
- SEU threshold better than 30 MeV
- suitable for most space projects, LEO, GEO or POLAR orbits and deep space,
- advance very low power 0.6 µm CMOS
- total dose effect simulation through Kd
- dedicated space design rules checkers

Basic Flow

The MG1RT design flow follows the standard MG1 one, with specific space design rules which can be verified with dedicated space design rules checkers.

The simulation tools allow to verify that under any level of total dose up to 100 Krad, the functionality and the speed performances are still met.

Because of the smaller size of the market for space application, the focus has been put on a limited number of base matrices, as follows :

- MG1014E, MG1042E, MG1090E, MG1140E and MG1265E.

The packages offering takes benefit of what has already been set for the MCRT and is as follows :

- multi layers quad flat package with up to 256 pins, J, gull wing or flat leaded,
- side brazed technology with up to 64 pins.

Under specific commercial conditions to be agreed on, some plastic packages can be considered : contact the factory.

So as to allow efficient design flow at both component and system levels, TEMIC has set an efficient route from the prototyping for A or B models, to flight models representative for EQM, delivering.

After negotiation, TEMIC can also offer a full service for :

- either a radiation evaluation on a batch per batch basis,
- or a radiation lot acceptance test (RLAT)

Finally, and as a natural consequence of our "dual use technology", for the purpose of better silicon usage efficiency and better performances, our composite MG1M offering is also available for space applications with the same features and capabilities as our "MG1M" and "MG1RT" offerings, but as a full custom service.

An hardened version of the MG1RT, called the MG1RT+, allowing to meet 100-200 Krad total dose and 50 MeV SEU levels, will be introduced during the second half of 96 : it will be library compatible with the MG1 and MG1RT ones (the difference being only on the propagation delays resulting from the characterization with the hardened process), allowing a new fluent route to upgrade any available designs, on MG1 or MG1RT, above 100 Krad total dose and 50 MeV SEU levels.

Arrays

MC 0.8 µm CMOS Gate Array

This document presents an overview of MC characteristics. For further information, a full datasheet can be provided upon request.

Description

MC gate arrays are a CMOS 0.8 µm, 2 metal layers gate array family ranging from 400 gates up to 66 kgates.

An original current controlled output buffer option is provided, to get a good compromise between speed and peak output current, and keep the noise figure low.

MC gate arrays exhibit a very good immunity to latch-up, through the use of an epitaxial P-type substrate.

Features

- CMOS technology – 2 metal layers
- 0.8 µm effective channel length
- 400 gates to 66 000 gates
- Maximum utilization
  – 90 % up to 12 000 gates
  – 70 % up to 12 000 gates
  – 60 % up to 66 000 gates
- High speed performance :
  0.4 ns typical gate delay
  (NAND2 – Fanout2)
  150 MHz typical toggle frequency
- Low supply current :
  1 µA/gate/MHz (operating)
  0.4 nA/gate (stand-by)
- Radiation tolerant process available
- 3 or 5 V operation
- On chip power–on–reset and low power oscillator
- Flexible I/O configuration : input, output, three-state, VCC & VSS, oscillator.
- Optional D-latch in each I/O
- 3 output buffer options : fast, current control, slew rate control
- Programmable output drive from 3.2 to 12.8 mA (2 to 8 TTL loads), parallelism up to 48 mA
- Dedicated software for optimum memory integration
- ESD Class 2 & latch-up free
- Wide range of packages including CPGA, CQFP, SOIC, PLCC, CLCC, QFP, Wafer, Die.
- On chip RAM generator up to 2 000 bits in one block.

Product Outline

Type	Total Gates	Maximum Usable Gates	Total* Pads
MCT04K	364	330	32
MCT08K ●	792	720	44
MCT2K ●	2040	1800	68
MC5K●	4670	4200	88
MCT8K ●	7884	7100	128
MC10K ●	10000	9000	128
MCT12K ●	11656	10500	160
MCR22K ●	21600	15000	148
MCT29K ●	29050	20000	200
MCR35K ●	35340	24000	184
MCR50K ●	50666	35000	220
MCT66K	66000	46000	292

* includes 4 dedicated VDD & VSS corner pads.
● ESA (European Space Agency) : Qualified.

I/O Buffers

Several input or output buffers can be synchronized with a clock signal through an integrated D-latch. Data transfer can occur on the rising or falling edge.

Inputs

Each input can be programmed as TTL, CMOS, or Schmitt Trigger, with or without pull up/pull down resistor.

Outputs

Fast Output Buffer

Fast output buffers are able to source or sink at least 3.2, 6.4 or 12.8 mA (i.e. 2, 4 or 8 TTL loads) according to the option chosen.

Current control output buffer

These buffers have been designed to smooth high current spikes during output transitions, especially when high

speed operation is required, while maintaining a good switching performance.

At the beginning of an output transition, 1/3 of the total output power is applied to the load, until the output voltage reaches VCC/2. Then, the full output stage is activated to speed up the second half of the switching phase.

This auto-adaptive technique provides a very good compromise between noise and switching performance.

Slew rate control output buffer

In this mode, the P and N output transistors commands are delayed, so that they are never “ON” together, resulting in a low switching current and low noise. These buffers are dedicated to very high load drive.

Design Modes

Designers can achieve MC gate array designs using one of the following EDA tool : CADENCE, COMPASS, MENTOR, SYNOPSYS.

For each of these EDA tool, MHS provides a macro library containing the schematic, simulation models for design verification, logic & timing simulations, and netlist generation.

After layout, back annotation information including layout parasitic delays can be fed back to the workstation to cross check overall circuit performance.

Absolute Maximum Ratings

Ambient Temperature Under Bias (TA) :

Commercial . . . . . 0°C to 70°C
Industrial . . . . . –40°C to +85°C
Military . . . . . –55°C to +125°C
Automotive . . . . . –40°C to +125°C
Maximum Junction Temperature . . . . . 150° C
Storage Temperature . . . . . –65°C to + 150°C
Supply voltage VDD . . . . . –0.5 V to + 7 V
Input/Output Voltage . . . . . –0.5 V to VDD + 0.5 V

Stresses at or above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

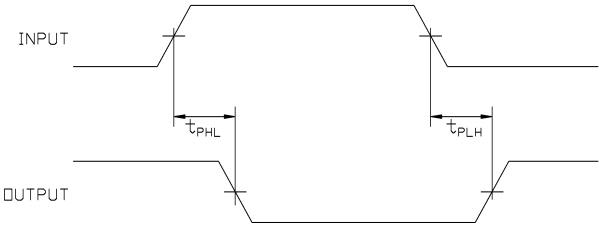
AC Characteristics

Specified at VDD = 5 V and TA = 25°C

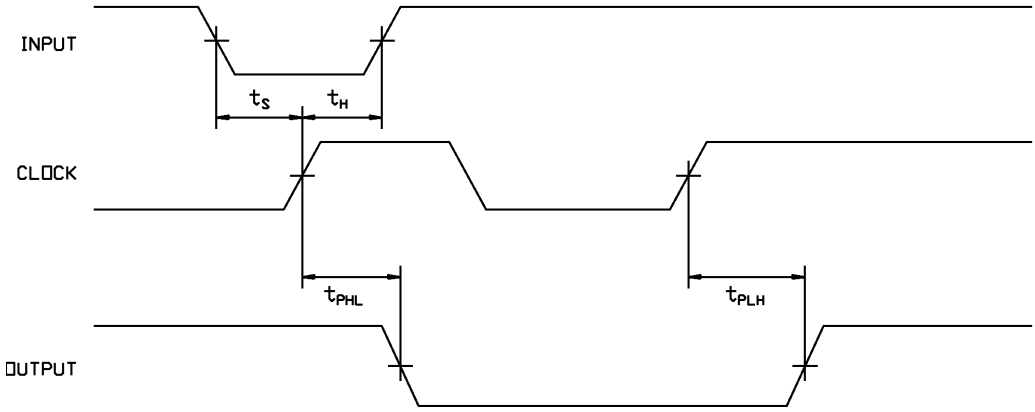
SYMBOL	MACRO	DESCRIPTION	TYPICAL PROPAGATION DELAY (ns) FANOUT		
			2	4	6
tPLH tPHL	NAND2	2–Input NAND	0.45 0.25	0.75 0.4	1 0.7
tPLH tPHL	BUFINTTL	TTL Input Buffer	1.15 1.25	1.3 1.35	1.5 1.45
tPLH tPHL	BUFINMOS	CMOS Input Buffer	0.9 0.75	1.1 0.85	1.3 0.95
tPLH tPHL tS tH	DFFR1	D Flip–Flop with positive Reset	1.55 1.45 0.5 0.5	1.85 1.55 0.5 0.5	2.15 1.65 0.5 0.5
tPLH tPHL tS tH		Input Buffer + D–Latch	1 0.8 0.5 0.5	1.5 1.1 0.5 0.5	1.9 1.4 0.5 0.5
			CAPACITIVE LOAD		
			50 pF	100 pF	200 pF
tPLH tPHL	BUFOUT	Fast Output Buffer	2.9 2.8	4..2 3.8	6.8 5.7
tPLH tPHL	BUCOUT	Current Control Output Buffer	7.5 6.5	12.7 10.2	
tPLH tPHL	BUDOUT	Slew Rate Control Output Buffer			16.5 12.4

Timing Diagrams

Inverting Gate



Flip-Flop



Propagation Delay Factors

Propagation delays are a function of several factors including fanout, interconnection capacitance, supply voltage, junction temperature, process tolerance, input transition time and polarity.

After layout, nominal delay values are obtained for (TA = 25°C, VDD = 5 V). The variation due to process tolerance is KP (KPmin = 0.7, KPmax = 1.4).

The propagation factors versus temperature and voltage are KT and KV respectively.

TEMPERATURE °C	KT
–55	0.64
–40	0.71
0	0.88
25	1
70	1.20
85	1.26
125	1.44

The actual propagation delay can be expressed as a function of the nominal delay :

$TP = KP \times KT \times KV \times TNOM$

Parameters KT and KV vary according to following table :

SUPPLY VOLTAGE VOLTS	KV
2.70	1.93
3.00	1.75
3.30	1.57
3.60	1.4
4.50	1.11
5.00	1
5.50	0.93

MC gate arrays Matrix/Package Availability

Package Type	Pins	Width	Lead Pitch	MC											
				T04K	T08K	T2K	5K	T8K	10K	T12K	R22K	T29K	R35K	R50K	R66K
PDIL	16	0.3	0.1	A	A										
	20	0.3	0.1	A	A	A									
	24	0.3	0.1	A	A	A									
	28	0.6	0.1	A	A	A	A	A	A	A					
	40	0.6	0.1		A	A	A	A	A	A	A				
SO	8		0.05	A											
	16		0.05	A	A	A									
	18		0.05	A	A	A									
	20		0.05	A	A	A	A								
	24		0.05		A	A	A								
	28		0.05		A	A	A								
PLCC J LEADED	28	0.45	0.05	A	A	A	A	A							
	44	0.65	0.05		A	A	A	A	A	A	A				
	68	0.95	0.05			A	A	A	A	A	A	A	A		
	84	1.15	0.05				A	A	A	A	A	A	A	A	A
PQFP	44	10x10	0.8		A	A	A	A	A						
	52						I	I	I						
	64						I	I	I	I					
	80	14x20	0.8				A	A	A	A	A				
	100	14x20	0.65					A	A	A	A	A	A		
	128	28x28	0.8						A	A	A	A	A		
	160	28x28	0.65						A	A	A	A	A	A	A
	208	28x28	0.5								A	A	A	A	A
	240													I	I
Power QUAD	80						A	A	A	A	A				
	100	14x20	0.65					A	A	A	A	A	A		
	128	28x28	0.8						A	A	A	A	A		
	144	28x28	0.65						I	I	I	I	I		
	160	28x28	0.65						A	A	A	A	A	A	A
	208	28x28	0.5								A	A	A	A	A
	240	32x32	0.5											I	I
	304	40x40	0.5											I	I
TQFP (1.4mm max)	44	10x10	0.8		A	A	A	A	A						
	52		0.5				I	I	I						
	64	10x10	0.65				I	I	I	I					
	80	14x14	0.5				A	A	A	A	A				
	100	14x14	0.5					A	A	A	A	A	A		
	128	20x20	0.5						A	A	A	A	A		
	144	20x20	0.65						A	A	A	A	A	A	A
	160	28x28													

A : Available. Contact MHS to check the pin out.
I : Introduction in progress (check for availability)

MCRT : Radiation Tolerant 0.8µm CMOS Gate Arrays

Description

TEMIC / MATRA MHS is the first European supplier for space application sub-micronic radiation tolerant CMOS gate arrays.

This is why TEMIC keeps offering a fluent way of moving up and down the quality and the space/radiation tolerant capability of its products offering, and makes available its advanced submicronic CMOS MC gate arrays family, through a mask compatible space / radiation tolerant process, so called “MCRT” : this is the result of the TEMIC “Dual Use Technology” strategy serving the AMS (Avionics, Military & Space) market segments.

It offers the user to either go directly to a radiation tolerant prototypes and flight models delivery, or to start with cheaper non radiation tolerant prototypes, converting, then, to the radiation tolerant version, only when EQM or FM are actually needed, provided proper simulations have been run before going either way.

Features

- mask compatible radiation tolerant version of the MC gate arrays family
- total dose capability, when tested at 1600 rad/h :
  - better than 100 Krads for functionality
  - 45 to 60 Krads for first stand by current drift
- no rebound effect demonstrated after annealing
- positive influence of space very low dose rate (< 1 rad/h)
- latch up free : better than 116 MeV
- SEU threshold better than 50 MeV
- suitable for most space projects, LEO, GEO or POLAR orbits and deep space,
- advance very low power 0.8µm CMOS process
- ESA qualified
- total dose effect simulation through Kd
- dedicated space design rules checkers

Basic Flow

The MCRT design flow follows the standard MC one, with specific space design rules which can be verified with dedicated space design rules checkers.

The simulation tools allow to verify that under any level of total dose up to 85 Krad, the functionality and the speed performances are still met.

When designs are considered to be procured at MIL-STD-883 level B at the best, the whole family of matrices can be considered (up to the MCT66KE on request : the E stands for the RT version).

When it is to be procured to more stringent quality flows (MIL-STD-883 class S or SCC9000 level B for instance), then a restriction shows up because of the die size, limiting the use of matrices to the MCT66KE, at the best.

You may also be willing to make designs falling into the capability domain of the ESA qualification : then a PID describes it, which allows to consider :

- the use of matrices up to MCR50KE at the best,
- packages with the following technologies and pin count :
  - multi layers quad flat package with up to 196 pins, J, gull wing or flat leaded,
  - side brazed technology with up to 64 pins.

So as to allow efficient design flow at both component and system levels, TEMIC has set an efficient route from the prototyping for A or B models, to flight models representative for EQM, delivering.

After negotiation, TEMIC can also offer a full service for :

- either a radiation evaluation on a batch per batch basis,
- or a radiation lot acceptance test (RLAT).

Finally, and as a natural consequence of our “dual use technology”, for the purpose of better silicon usage efficiency and better performances, our composite MCM offering is also available for space applications with the same features and capabilities as our “MCM” and “MCRT” offerings under the “MCMRT” name.

Composite Arrays

MG1M 0.6 µm CMOS Composite Arrays

This document presents an overview of MG1M characteristics. For further information, a full datasheet can be provided upon request.

Description

MG1M Composite Array is an enhanced embedded array generator fully compatible with MG1 Gate Array serie, offering the best trade-off between design cost and integration efficiency.

A very high integration density is achieved, close to the one obtained through a cell–based approach, while keeping the advantages -flexibility, cycle time of gate arrays.

Building a Composite Array consists in associating on the same chip, gate arrays and optimized blocks. This allows a creation of dedicated architectures which can be common to several applications by only changing the customization levels of the array.

Powerful and flexible generators are provided : RAM, ROM, gates, multipliers, adders...)
Optimized blocks as cell–based, standard products or full custom blocks can be imported. The gate array section is designed through standard MG1M gate array design package running on workstation.

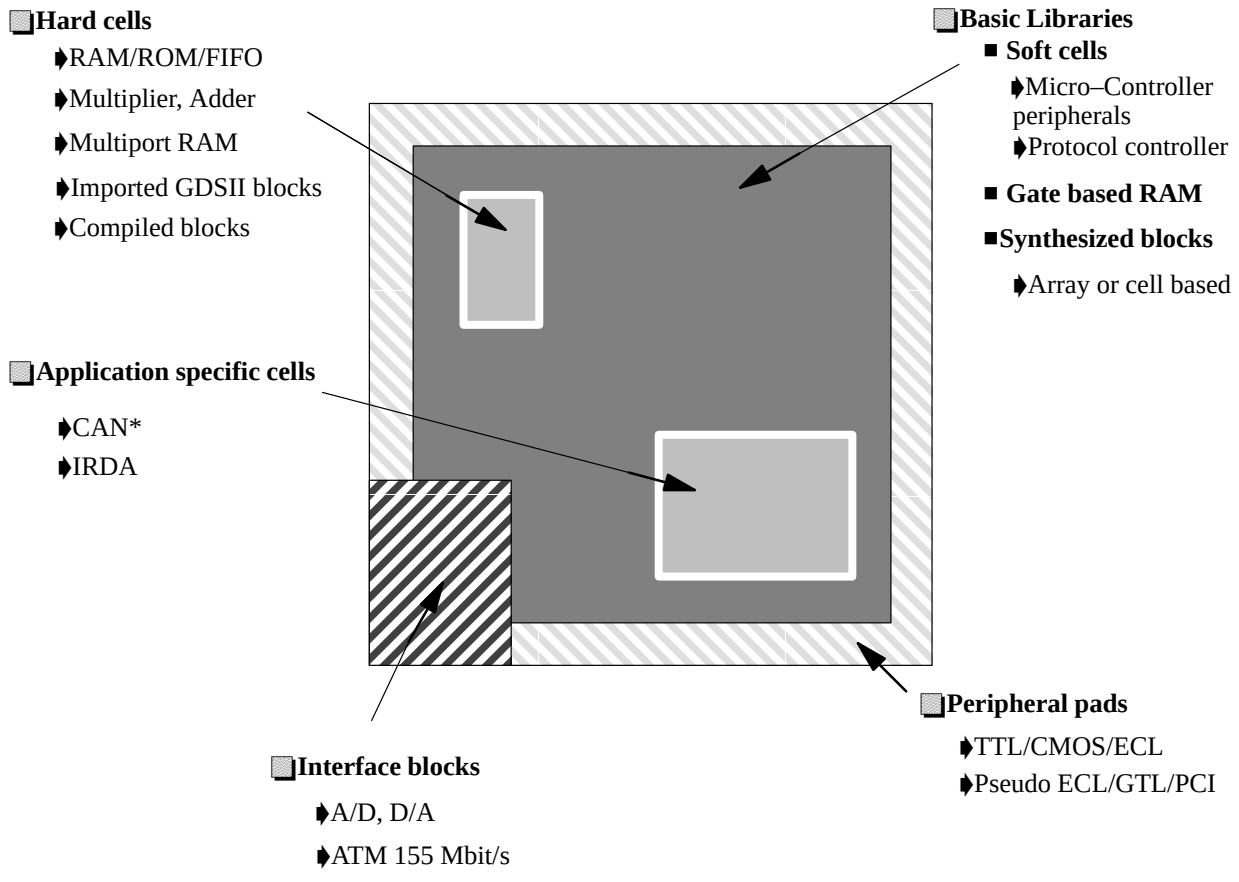
The composite array topology is shown fig. 1.

Features

- RAM, DPRAM, FIFO Compilers with almost same integration level and speed than standard memories and more flexibility
- Library Optimised for Synthesis, Floor Plan & Automatic Test Generation (ATG)
- High Speed Performances :
  – 250 ps Typical Gate Delay
  – 350 MHz Toggle Frequency
- High System Frequency Skew Control :
  – 250 MHz PLL for Clock Generation
  – Clock Tree Synthesis Software
- 3 & 5 Volts Operation; Single or Dual Supply Modes
- Low Power Consumption :
  – 0.9 µW/Gate/MHz @3 V
  – 2.4 µW/Gate/MHz @5 V
- Integrated Power on Reset
- Versatile I/O Cell : Input, Output, Bidirectionnal, Supply, Oscillator
- Standard 12mA I/Os, parallelism up to 48 mA
- ESD (2 kV) and Latch-up Protected I/O
- CMOS 0.6 micron – 3 metal layers
- CMOS / TTL / ECL / GTL / PCI Interface
- High Noise & EMC Immunity :
  – I/O with Slew Rate Control
  – Internal Decoupling
  – Signal Filtering between Periphery & Core
  – Application Dependent Supply Routing & Several Independent Supply Sources
- Wide Range of Packages Including CPGA, CQFP, SOIC, PLCC , CLCC, PQFP, Wafer, Die
- Advanced CAD Support : Floor Plan, Proprietary Delay Models, Timing Driven Layout, Power Management
- Cadence, COMPASS, Mentor, Synopsys Reference Platforms
- EDIF & VHDL Reference Formats
- Upward Compatibility With MC & MF Gate Arrays, MCM & MFM Composite Arrays.
- Full Compatibility with MG1 Composite Sea of Gates Series
- Available In Commercial, Industrial, Automotive, Military & Space Quality Grades
- Special Versions on Radiation Tolerant Process

Topology

Figure 1. Composite Array CMOS 0.8 µm



* Under development

Composite Arrays

Product Outline

Embedded Arrays are generated on request through a discussion between Customer and MHS Design Centers

Libraries

The MG1M cell library has been designed to take full advantage of the features offered by both logic and test synthesis tools.

Cell / Macrocells libraries

5 and 3 Volt libraries can be delivered.

Macros library

Design testability is assured by the full support of SCAN, JTAG (IEEE 1149) and BIST methodologies.

I/O Libraries

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator is located close to each buffer.

Memory Generators

RAMLIB is an heterogeneous memory plan generator used to customised “intelligent ”memory blocks to speed up Data Transmission and Pattern recognition algorithm (Protocol handling....).

Specification is done by customer and RAMLIB automatically generates decoding, interface, layout and VHDL model.

Typical basic cells are :

- DPRAM
- DPRAM with Reset
- DPRAM with asynchronous output
- DPRAM with set on port 1, reset on port 2, Async output
- DPRAM with set or reset from port 1 and inverted open drain output with enable
- DPRAM with comparison on port 1 with masking
- MASK RAM cell
- RAM with reset and async outputs
- RAM to drive output enable
- RAM with comparison
- RAM with comparison and reset
- RAM with comparison to external value or 1
- 64 wordline address decoder
- Wordline driver for DPRAM and RAM
- Bitline multiplexer and address decoder
- Write amplifier
- Sense block for comparison
- Precharge block

Clock generation & PLL

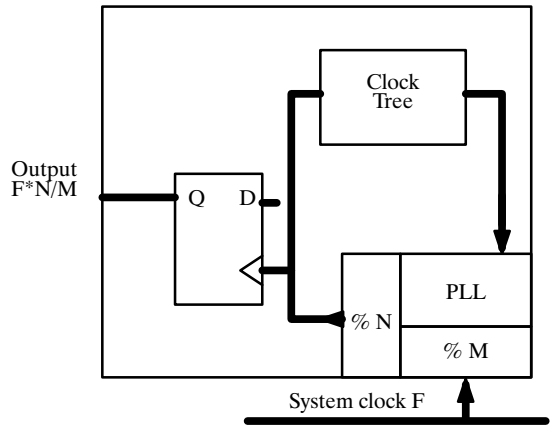
Clock generation

TEMIC / MHS offers 4 different types of oscillators : low power 32KHz crystal oscillator, high frequency crystal oscillator and 2 RC oscillators. For all devices, the mark-space ratio is better than 40/60 and the start-up time less than 10 ms; the other characteristics are summarized below :

	Frequency (MHz)		Typical consumption (µA)
	Minimum	Maximum	
Xtal 32K	0.03	0.034	50
Xtal 50 M	2	50	1 000
RC 10M	0.02	10	600
RC 32 M	10	32	1 500

PLL

Two independent PLL devices are located in upper left and lower right corners. Each may be used for the following functions :



The maximum frequency at PLL input after division by M is 70 MHz.

The maximum internal clock frequency is 250 MHz at 5 V and 150 MHz at 3 V; the minimum frequency is 20 MHz.

AC Characteristics examples

Specified at VDD = +5 V, TJ = 25°C, Process typical (all values in ns)

Description	Transition	Load (pf)		
		20	40	60
Output buffer with 12 mA drive	Tplh	1.85	2.69	3.54
	Tphl	1.45	1.82	2.19

Description	Transition	Standard Loads		
		2	5	10
2-Input NAND gate	Tplh	0.31	0.49	0.78
	Tphl	0.19	0.27	0.41

Specified at VDD = +3 V, TJ = 25°C, Process typical (all values in ns)

Description	Transition	Load (pf)		
		20	40	60
Output buffer with 12 mA drive	Tplh	3.05	4.44	5.84
	Tphl	2.39	3.00	3.61

Description	Transition	Standard Loads		
		2	5	10
2-Input NAND gate	Tplh	0.40	0.65	1.07
	Tphl	0.27	0.39	0.59

Composite Arrays

Propagation delays

Propagation delays for MG1 cells and blocks are a function of several factors including fan out, signal slope, interconnection capacitance, supply voltage, junction temperature and process tolerance and additionaly total irradiation dose for special operating conditions.

Propagation delays are provided for MG1 cells under nominal conditions (Tj = 25°C, VDD = 5.0 or 3.0 V, typical process, no irradiation). Worst case values are obtained by applying derating coefficients for temperature, voltage, process and total dose irradiation : KT, KV KP and KD. These coefficients are also design dependent and in the design kits each cell has its individual set of parameters.

Worst case propagation delays can however be estimated by using the following formula and tables :

Worst case = Typical * KTmax * KVmax * KPmax (* KDmax)

Voltage	KV
4.5	1.1
5	1
5.5	0.95

Process	KP
Best	0.82
Typical	1
Worst	1.28

Voltage	KV
2.7	1.15
3	1
3.3	0.89
3.6	0.81

Temperature	KT
–55	0.75
–40	0.79
0	0.92
25	1
100	1.24
115	1.29
145	1.38

Dose (krad)	KD
0	1
tbd	tbd

Absolute Maximum Ratings

Ambient temperature under bias (TA)
Commercial . . . . . 0°C to +70°C
Industrial . . . . . –40 to +85°C
Automotive . . . . . –40 to +125°C
Military . . . . . –55 to +125°C
Maximum Junction temperature . . . . . 150°C
Storage temperature . . . . . –65 to + 150°C

TTL/CMOS :
Supply voltage VDD . . . . . –0.5 V to +7 V
I/O voltage . . . . . –0.5 V to VDD + 0.5 V
Stresses at or above those listed may cause permanent damage to the device.
Exposure to absolute maximum rating conditions for extended period may affect device reliability.

Packaging

TEMIC / MHS offers a wide range of packaging options. For packaging requirements other than listed below, and to check availability of a given composite array in a given package, please contact your TEMIC representative.

Plastic Package Type	Pin Number (Leads)																
	24	28	32	40	44	52	64	68	80	84	100	128	144	160	208	240	304
DIL	X	X		X													
PLCC		X			X			X		X							
SO	X	X	X														
PQFP					X	X	X		X		X	X		X	X	X	X
Power QUAD					X				X		X	X		X	X	X	X
VQFP/TQFP					X	X	X		X		X		X				

Die form and Tab	Pin Number (Leads)
Wafer	Over 300 leads
Die	Over 300 leads
TAB	Over 300 leads

MCM 0.8µm Composite Arrays

This document presents an overview of MCM characteristics. For further information, a full datasheet can be provided upon request.

Description

MCM Composite Array are an enhanced embedded array generator fully compatible with MC Gate Array, offering the best trade-off between design cost and integration efficiency.

A very high integration density is achieved, close to the one obtained through a cell–based approach, while keeping the advantages -flexibility, cycle time of gate arrays.

Building a Composite Array consists in associating on the same chip, gate arrays and optimized blocks. This allows a creation of dedicated architectures which can be common to several applications by only changing the 4 customization levels of the array.

Powerful and flexible generators are provided : RAM, ROM, gates, multipliers, adders...)
Optimized blocks as cell–based, standard products or full custom blocks can be imported. The gate array section is designed through standard MC gate array design package running on workstation.

The composite array topology is shown fig. 1.

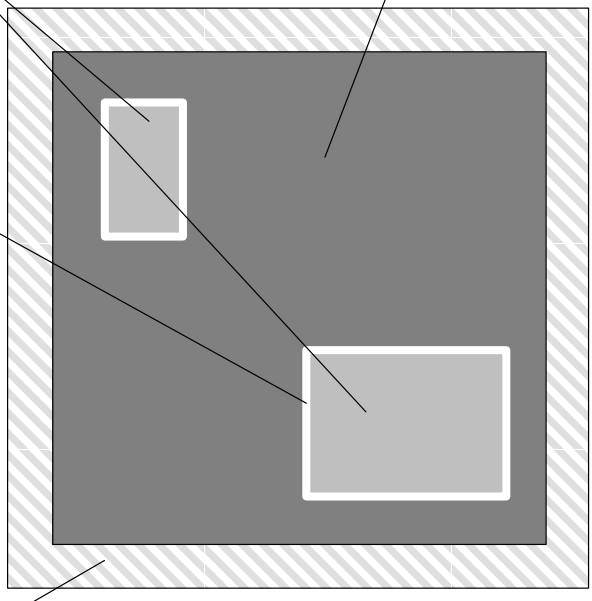
Features

- Enhanced Array generator compatible with MC
- CMOS technology – 2 metal layers
- 0.8 µm effective channel length
- Radiation tolerant process available
- High integration
  - Megablocks from customer or MHS library including RAM/ROM, data path, protocol converter etc.
  - Gate array for extra logic and macros
- Flexible memory integration
  - Variable size and organization
  - Up to 64 kbit ROM and static RAM
- High speed performance
  - 0.4 ns typical gate delay
  - 150 MHz typical toggle frequency
  - RAM 64 kbit, 29 ns cycle time
  - ROM 64 kbit, 65 ns cycle time
- Low supply current
  - 1 µA/gate/MHz (operating)
  - 0.4 nA/gate (stand-by)
- Flexible I/O configuration : input, output, three-state, VCC & VSS
- Optionnal D-latch in each I/O
- 3 output buffer options : fast, current control, slew rate control
- Programmable output drive from 3.2 to 12.8 mA (2 to 8 TTL loads), parallelism up to 48 mA
- 3 or 5 V operation
- On chip power on reset and low power oscillator
- Wide range of packages including CPGA, CQFP, SOIC, PLCC, QFP, Wafer, Die
- ESD class 2 & latch-up free

Composite Arrays

Topology

Figure 1. Composite Array CMOS 0.8 µm



- **Cells : Optimised for Automatic synthesis**
- **Macrocells**
  - Coder, decoder
  - Arithmetic function
  - Counter, register...
- **MEGA Cells**
  - Microcontroller peripherals (8251, 59, ...)
  - Protocol controllers (X21, I2C, V110, V120, ...)
  - UART
- **Gate based RAM generator**
- **Synthetised blocks**

- **Hard blocks**
  - RAM/ROM
  - Multiplier, Adder
  - Multiport RAM
  - Imported GDS II blocks
  - Compiled blocks

- **Application specific cells**
  - ABUS,VAN,CAN*
  - CAM, Smart RAMs
  - AAL*, CRC*

- **Interface blocks**
  - A/D, D/A

* under development

Megablocks

The Megablocks can be hard blocks from MHS or customer development.

RAM : The synchronous RAM cell offer fully static operation and low power consumption.
The smallest RAM which can be generated is a 32×1 and the largest 2048×8 or 1024×16. (in one block)
The minimum cycle time for the 32×1 bit memory is 22 ns and for 1024×16 bit 29 ns. Two synchronous RAM blocks can be derived from the standard TEMIC / MHS products. (64kBit and 32kBit blocks, 30 ns access time, which can be formated by 1,4 and 8 for example)

ROM : The sizes for the ROM array can vary in range of 128 to 32768 words with word format from 32 to 2 bits, respectively. The cycle time for 64 Kbit memory is 65 ns.

ALU : The 29101 full custom block for composite arrays is a 16-Bit “bit slice” ALU which has functionalities equivalent to 2901 or 2902 carry-look-ahead generator.

MULTIPLIERS : The multipliers generator performs multiplications of two operands in two’s complement format. The multipliers can be optimized for speed or area. The range of the operands is 8 to 64. Latches can be added to the outputs and inputs. Typical performance for 16 $\times$ 16 multiplication (+ 25°C and + 5 V) is 18 ns and typical power consumption is 2.6 mW/ MHz.

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VDD & VSS Requirements

High speed operation of the output buffers puts stringent requirements on the number of power supply pads, to avoid the generation of internal current spikes as the buffers charge and discharge the external loads.

To provide clean supply rails for the internal matrix, two types of supply are provided :

– VCCA and VSSA for the internal logic
– VCCB and VSSB for the buffers

Each output buffer must be used within a range of “n” positions from a supply pad (VCC and VSS).
Fast Output Buffer : n = 4 for the fastest option
Current Control Output Buffer : n = 20
Slew Rate Control Output Buffer : n = 6 to 14.

I/O Pads programmable will be used to create additional supply pads whenever required.

A functional test program is automatically generated from the simulation results, and test coverage evaluated.

Once MHS and customer agree on the results, a design review meeting is set up to release last layers generation and samples fabrication, assembly and test.

Production will begin after MHS has received a written agreement of the samples operation.

Composite Arrays

MCM Composite Array

Composite Array Matrixes Examples

Name	Contents	Physical/ Usable Gates	Pads
MCM32K5	2 × 1024 × 16 RAM (GDT)	6792/4754	148
MCM1HK6	16 bits ALU	5571/3899	100
MCM32K18	2 × 1024 × 16 RAM (GDT)	18744/13120	176
TCM1HK23	2048 × 8 asynch RAM	23932/16752	220
MCM1HK4	1 × VAN DLC hardblock (29C461B)	4881/3417	108
MCM16K25	2 × 512 × 16 RAM, 24 × 16 MULT	25122/~17600	196
MCM1HK8	2K × 8 DPRAM	7946/~5500	136
TCM1HK7	1 72 × 68 com. matrix (GDT)	7695/~5386	192

Packaging

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Plastic Package Type	Pin Number (Leads)																
	24	28	32	40	44	52	64	68	80	84	100	128	144	160	208	240	304
DIL	X	X		X													
PLCC		X			X			X		X							
SO	X	X	X														
PQFP					X	X	X		X		X	X		X	X	X	X
Power QUAD					X				X		X	X		X	X	X	X
VQFP/TQFP					X	X	X		X		X		X				

Die form and Tab	Pin Number (Leads)
Wafer	Over 300 leads
Die	Over 300 leads
TAB	Over 300 leads

Ordering Information

Consult your TEMIC sales office.

Design Flows

Design Offering

Five different ASIC design offerings are available : ULC, Gate Arrays, Composite Arrays, Cell Based and Full Custom, each physical implementation giving an answer to the compromise : flexibility/unit price and integration/development cost.

Design Modes

Three different design modes can be agreed between Customer and MHS, depending on system and integration skills requirements.

Mode	Logic Design	Physical Layout	Design Tools
Customer Design	Customer	Customer	Customer tools
Customer and TEMIC Design	Customer	MHS	MHS supported tools (Netlist and simulation)
TEMIC Design	MHS	MHS	MHS supported tools (Netlist and simulation)

Supported tools are currently CADENCE, COMPASS, MENTOR, SYNOPSYS and VHDL/VITAL.

Design Modes versus Design Offering

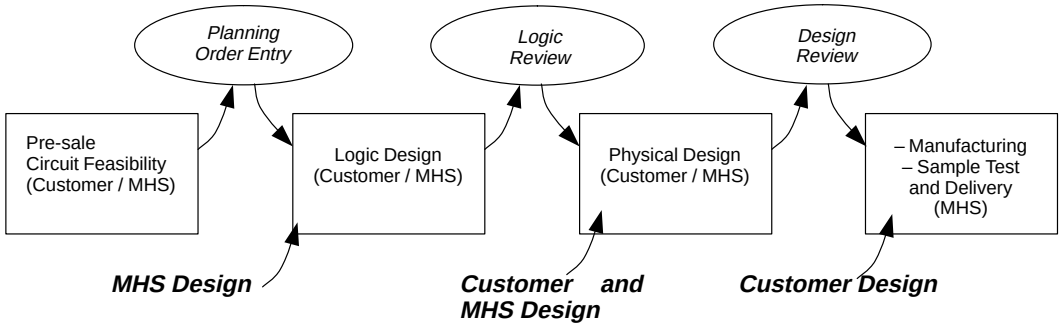
Offering \ Mode	Customer Design	Customer and MHS Design	MHS Design
ULC			□
Gate Array		x	□
Composite Array		x	□
Cell Based	x	○	□
Full Custom	x		

x : standard offer.
○ : depending on human and hardware ressources needed and/or available.
□ : specific development using MHS own expertise.

Design Phases and Meetings

The design of a circuit is separated into four main phases, separated by three major meetings between MHS and the Customer, as shown in Figure 1.

Figure 2. The design phases and meetings.



Digital Integration

Processes

Description

MHS develops a wide range of CMOS processes, used for catalog products or ASICs' volume production. Their common features are high performance / high speed both with low power consumption, either in stand–by or operating modes.

MHS/TEMIC makes those processes available for selected customers/partners for their own design.

Features

	Technology	Well	Lithography (µm)	Poly Layers	Metal Layers	Operating Voltage (VO)	Characteristics
Digital Series							
FCC1D	CMOS	N	0.8	1	2	5 or 3	
FCC1S	CMOS	N	0.8	1	1	5 or 3	
FCC2D	CMOS	Twin	0.6	1	2	5 and/or 3	
FCC2T	CMOS	Twin	0.6	1	3	5 and/or 3	
FCB1D	BICMOS	Twin	0.8	1	2	5 and/or 3	NPN
Mixed Analog / Digital Series							
FCA1D	CMOS	N	0.8	2	2	5 and/or 3	
FCA2D (1)	CMOS	N	0.6	2	2	5 and/or 3	Low V_t
FCA2T (2)	CMOS		0.6	2	3	5 and/or 3	
Non Volatile Series							
FCN1D	CMOS	2	0.8	1	2	5	EPROM
FCN2D (1)	CMOS	2	0.6	1	2	5 and/or 3	EPROM
FCN2T (2)	CMOS	2	0.6	1	3	5 and/or 3	
Radiation Tolerant Series							
FCT1D	CMOS	N	0.8	1	2	5	Guard Ring
FCBTD	BICMOS	Twin	0.8	1	2	5	Guard Ring
FCT2D	CMOS	Twin	0.6	1	3	5 and/or 3	Guard Ring

(1) Under Development (2) Planned

MHS Processes include digital CMOS processes and several derivatives done from the CMOS core basis :

- mixed analog/digital series with one more polysilicon layer and low V_t transistors
- non volatile series with high voltage NMOS transistors and programming/sensing/erasing capabilities
- radiation tolerant process with specific guard rings